

## REMARKS

In view of the above amendments and following remarks, reconsideration and further examination are requested.

In the Final Rejection mailed November 18, 2005: claims 27, 29 and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Buchwalter et al.; claim 27 was rejected under 35 U.S.C. § 102(b) as being anticipated by Lee; claims 28 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Buchwalter et al. in view of Wu and Yang; claims 28-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Wu and Yang; and claims 15-17, 22, 24, 26, 33 and 35-65 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of Ohno and further in view of Yang.

On February 21, 2006, a reply was filed in response to the Final Rejection. On April 21, 2006, an Advisory Action was mailed. This Advisory Action indicated that certain of the rejections as expressed in the Final Rejection would be withdrawn, while other of the rejections would be maintained. Specifically, claim 27 remains rejected under 35 U.S.C. § 102(b) as being anticipated by Lee; claims 28-31 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Wu and Yang; and claims 15-17, 22, 24, 26, 33 and 35-65 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu in view of Ohno and further in view of Yang. These rejections are respectfully traversed, and the relied-upon references are not applicable with regard to the currently presented claims for the following reasons.

Initially the Examiner's reliance on Lee to reject independent claims 27 and 29 will be addressed. Claims 27 and 29 each recite a method for forming a semiconductor device comprising, in part, forming contact holes **to a uniform depth** through a first dielectric film and a second dielectric film. In order to read this limitation on Lee, the Examiner stated in the Advisory Action that, with regard to Lee,

although the vias are not explicitly shown, *if* the vias were made to connect through the first and second dielectric layers to the source/drain contacts, then the figures show that these portions of the dielectric layers have uniform thicknesses.

It is not disputed that in Lee holes can be formed to a uniform depth through first and second dielectric films; however, this is not sufficient to support the rejections based on Lee. In this regard, a reference can only be used for that which it actually or inferentially teaches, and cannot be relied upon for a teaching that is merely possible or speculative. While Lee does disclose forming vias, Lee fails to teach or suggest forming these vias to a uniform depth as recited in claims 27 and 29.

Specifically, Lee discloses that a top dielectric layer 50 is deposited on dielectric layers 46 and 48 which cover stripes 20, 24 and 42 as shown in Fig. 7D, and subsequently, vias are formed in the dielectric layers 46 and 48 (column 5, lines 4-6). Since the vias are formed in this sequence, the vias penetrate through the top dielectric layer 50 to the dielectric layers 46 and 48. And, if this via forming procedure is applied in the process represented by Figs. 9D or 10C of Lee, in accordance with the Examiner's indication in the Advisory Action, then vias would be formed so as to penetrate through the top dielectric layer 50 to somewhere in the dielectric layer 52. However, Lee is silent as to which elements in the semiconductor device are connected to each other by the vias, and Lee is also silent as to the location and/or dimensions of the vias. As such, Lee does not disclose, either expressly or implicitly, forming contact holes to a uniform depth. Neither Wu nor Yang resolve this deficiency of Lee.

Thus, claim 27 is not anticipated by Lee, and claim 29 is not obvious over a combination of Lee, Wu and Yang. Accordingly, claims 27 and 29, as well as claims 28, 30, 31, 50, 51, 61 and 62 which depend therefrom, are allowable.

The following is provided to address the rejection based on a combination of Wu, Ohno and Yang.

Independent claims 15, 32, 35 and 53 have been amended so as to clearly recite forming the first dielectric film **as a single layer on a substrate so that the first dielectric film fills entire spaces between gate electrodes (interconnections)**. A combination of Ohno, Wu and Yang fails to disclose or suggest this feature of claims 15, 32, 35 and 53.

With regard to Ohno, this reference discloses in Figs. 10B-15 a method for forming a semiconductor device, wherein two different dielectric films, i.e., an etching-stop layer 40 and an

insulating interlayer 41, are formed between adjacent gate electrodes 14B in a region of logic circuit on semiconductor substrate 10. Similarly, Ohno discloses in Figs. 10A-16 that two different dielectric films, i.e., first and second insulating material layers 18 and 19, are formed between adjacent gate electrodes in a region of DRAM. Accordingly, because of these two films or layers between adjacent gate electrodes, neither of these films or layers can fill **entire spaces** between these adjacent gate electrodes.

With regard to Wu, this reference discloses in Fig. 9 that two different dielectric films 38 and 52 are formed between adjacent gate electrodes 34, whereby neither of these films can fill entire spaces between these gate electrodes. Similarly, in Yang there are layers 16 and 20 between adjacent interconnecting lines 14.

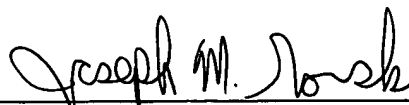
Thus, the combination of Ohno, Wu and Yang fails to disclose or suggest forming a first dielectric film **as a single layer so that the first dielectric film fills entire spaces between gate electrodes (interconnections)**, and therefore fails to render obvious the present invention as recited in claims 15, 32, 35 and 53. Accordingly, claims 15, 32, 35 and 53, as well as claims which depend therefrom, are allowable.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in condition for allowance and an early Notice of Allowance is earnestly solicited.

If after reviewing this Amendment, the Examiner believes that any issues remain which must be resolved before the application can be passed to issue, the Examiner is invited to contact the Applicant's undersigned representative by telephone to resolve such issues.

Respectfully submitted,

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